Development and test operation of the prototype of the new beam interlock system for machine protection of RIBF

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Continuing from 2021, we are developing a new beam interlock system (BIS) for machine protection based on CompactRIO[1] (hereafter, cRIO-BIS), a product by National Instruments, as a successor system to the BIS,[2] which has been in operation since 2006. We set up a prototype using one CompactRIO and one expansion chassis with I/O modules and developed the logic for digital input signals. The prototype signals for both a beam chopper and a beam stopper (Faraday cup) immediately after receiving an alert signal. Details are shown in Fig. 1.

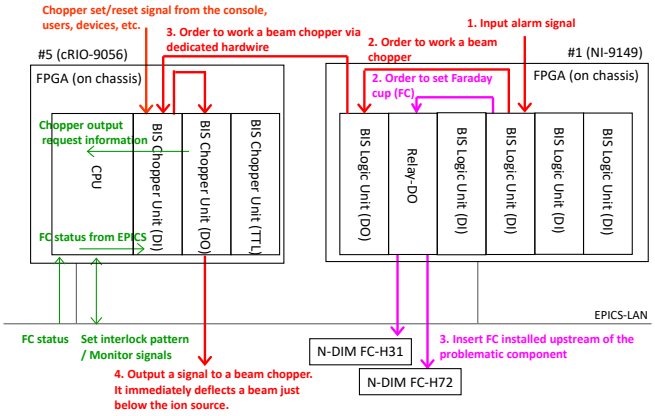

Fig. 1. Hardware configuration and process flow in the cRIO-BIS prototype.

The CompactRIO system has three layers for implementing logic for signal control: a field-programmable gate array (FPGA) layer, which is the most reliable and capable of the fastest signal processing, a real-time OS (RT-OS) layer that is positioned in the upper layer of FPGA and communicates with FPGA, and a Windows-OS layer that is positioned in the upper layer of them and communicates with them. FPGA is implemented on both CompactRIO and its expansion chassis, and RT-OS is implemented on CompactRIO. The goal of cRIO-BIS is to stop the beam within 1 ms by outputting a signal to the beam chopper from an alert signal input. Thus, interlock logic for signal input/output is implemented on the FPGA. However, signal condition setting and monitoring do not require the same speed as interlock logic. Thus, they are implemented on the RT-OS and controlled by using experimental physics and industrial control system (EPICS)[3] by setting up an EPICS server on the RT-OS.

Based on the operational experience of the BIS, cRIO-BIS implements two types of logic units; BIS Logic Unit (BLU) and BIS Chopper Unit (BCU). The BLU judges conditions such as mask and holding time for alert signal input and sends a signal to the BCU to request a signal to the beam chopper via dedicated hard wire. The BCU compares the input signal from the BLU and the insertion status of the Faraday cup and outputs a signal to the beam chopper. Since the BCU is designed to perform not only the function of BIS but also the role of the existing chopper signal control panel (it will be decommissioned in the future), it also receives signals from the console's manual switches and user's devices and outputs signal to the beam chopper.

After developing the prototype in the control room, its two stations were installed next to RIBF-BIS station 5 in the computer room of the Nishina Building and next to RIBF-BIS station 1 in the power supply room 2 of the RIBF building. The signal wiring was performed during the summer maintenance period. Since the prototype was planned to be tested in a part of the RIBF-BIS consisting of 5 stations, we connected the input signals into the prototype in parallel with the RIBF-BIS and evaluated its performance. The GUI for signal settings and prototype monitoring has been developed using the Control System Studio (CSS)[4] of EPICS, and the log system has been developed using the system in RILAC-operation.[5]

After installing the prototype, we measured the response time of the system with alert signals generated experimentally from an actual component and obtained a result of approximately 250 μs (between 229.0 μs to 260.0 μs). This is consistent with the system's response time measurements using test input signals in the control room. Furthermore, it was confirmed by the test that the response time could be reduced to less than 200 μs by adding a pull-up circuit to the signal input/output part. Since the response time of RIBF-BIS measured using the same signal was approximately 15 ms, we were able to develop a system that is approximately 100 times faster than the BIS.

We have started the test operation of the prototype during the beam service times scheduled in the latter half of the fiscal year 2022. Some minor corrections were necessary; however, no major defects were observed.

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References

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