Development of a low-cost FPGA-Integrated TDC

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The time-to-digital converter (TDC) is an indispensable instrument to measure timing information in physics experiments. In recent years, the TDC has been implemented in various methods using FPGAs and ASICs.[1] The tapped delay-line method is widely used to obtain an excellent timing resolution.[2,3] However, this method is disadvantageous in terms of cost because it consumes a large number of logic gates. In contract, the multi-phase clock method is suitable for many-channel systems with a moderate resolution.[4]

In RIBF experiments, many-channel detectors are being developed to increase the rate tolerance of beam detection. For example, SR-PPAC[5] requires 152 TDC channels per detector, which has the timing resolution of 250 ps (σ). We have began to develop a low-cost FPGA-integrated TDC based on the multi-phase clock method for many-channel gaseous detectors such as PPACs and drift chambers.

The prototype TDC board is shown in Fig. 1, and it operates under the MPV system.[6] We adopted Xilinx XC7A35T-2FTG256I which is a cost-optimized FPGA, to implement the TDC function. This board accepts a low voltage differential signaling (LVDS) level only. Thus, the production cost was significantly suppressed. The specifications of TDC are as follows: 64-ch hit input, 4-ch control I/O (1 ch for trigger), 125-ps LSB, 64-us full scale range, multi-hit, leading and trailing edge detection.

The TDC function consists of course timing (2-ns steps) by using 500-MHz clock counter and fine timing (125-ps LSB) using the dedicated circuit shown in Fig. 2. Eight clocks with different phases of 22.5 degrees each are distributed to the entire FPGA through the clock lines that has the almost equal length. Using an invert component, each clock can be shifted by 180 degrees. A total of 16 multi-phase clocks are connected to the clock input

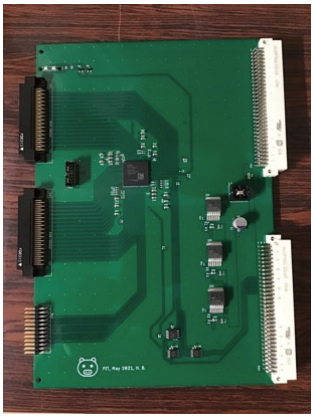

Fig. 1. Photo of the FPGA integrated TDC board.

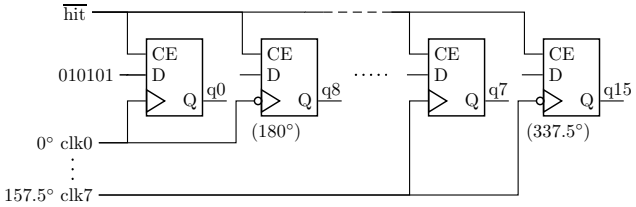

Fig. 2. Circuit diagram for fine timing.

ports of 16 flip-flops. To the D port (data), a signal that toggles 0→1→0→1 is input in sync with each clock. The inverted hit signals ($\overline{\text{hit}}$) are connected to the CE ports (clock enable). If CE is "1," output bits of q0–q15 are always toggling. When a hit occurs, *i.e.* CE is "0," these transitions are suspended. The bit pattern of q0–q15 determines the fine timing. For example, if the pattern is either "0000000000000111" or "1111111111110000," the fine timing is "4."

The multi-phase clocks are distributed to flip-flops through the clock lines with a small skew. Because the adopted FPGA has only 12 clock lines, wiring from the hit to each CE input should be manually configured to ensure that the propagation delay is as equal as possible. The variation of this delay determines the linearity of fine timing that affects the timing resolution. The differential non-linearity (DNL) and resolution for a typical channel was measured (Fig. 3). The timing resolution was 78.9 ps in σ, which is sufficient for many-channel gaseous detectors.

As shown in this report, we successfully confirmed the TDC functions. The implementation of the trigger processing is now in progress.

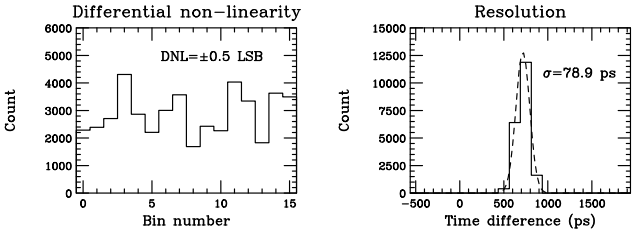

Fig. 3. Differential non-linearity and resolution.

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References

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