

Design of reliable control with star-topology fieldbus communication for an electron cyclotron resonance ion source at RIBF[†]

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A new superconducting electron cyclotron resonance ion source (SC-ECRIS) was installed at RILAC in the RIKEN project to increase the beam intensity.¹⁾ Considering the new SC-ECRIS, the control system should follow the current RIKEN 28-GHz SC-ECRIS control system for RILAC2, because the RIKEN 28-GHz SC-ECRIS control system based on Experimental Physics and Industrial Control System (EPICS) has proven to be successful.²⁾ Thus, in the new SC-ECRIS control system, we adopted a programmable logic controller (PLC) of the Yokogawa FA-M3V series.

However, the RIKEN 28-GHz SC-ECRIS control system is less reliable because it uses TCP/IP communication between the PLC controllers for interlock signal. In general, a network I/O-based interlock system is not highly reliable owing to the failure of network switch in the network route and slow signal transmission speed as compared to the bus access. Therefore, the reliability of a signal through TCP/IP is lower than that of an electric signal, which results in a less reliable interlock.

Accordingly, to overcome this disadvantage, a new SC-ECRIS control system has been designed by implementing two different types of CPUs in the main PLC station. Essentially, the sequence PLC CPU (F3SP71) in the first slot and Linux PLC CPU (F3RP61) in the second slot have been implemented in the same PLC base module. In the sequence PLC CPU, the sequential program called ladder program runs for the interlock system and the Linux CPU runs the EPICS input/output controller (IOC) and provides operation services to users via the EPICS Channel Access protocol. In the Yokogawa FA-M3V series, the fieldbus is called the FA bus. The controllers on the main station manage four substations connected through FA bus communication, electrically isolated by optical fibers. Because the heavy ions generated by an ion source are extracted to the low-energy beam transport by high voltage, substations also need to be implemented at the high-voltage stage in some cases. The new SC-ECRIS control system consists of a main PLC station and five PLC substations with star-topology fieldbus communication using optical FA bus modules (see Fig. 1). At present, this control system does not include the control for superconducting electromagnet power supplies. The system has been implemented by another

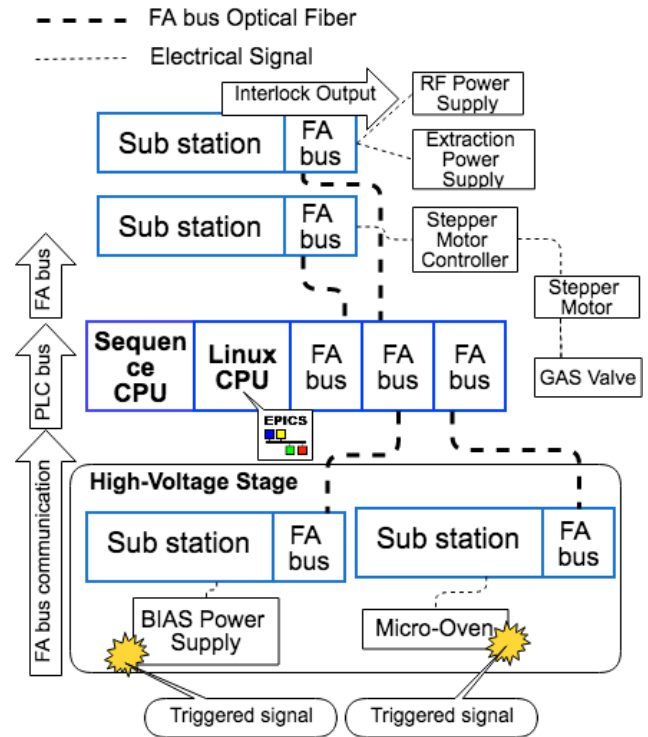


Fig. 1. System chart of new SC-ECRIS control system. Interlock signal is delivered by bus communications.

PLC with EPICS.

This new SC-ECRIS control system was successfully used in the test operation of the new SC-ECRIS performed in August 2018 without any serious problem. Because two CPUs were mounted in one base unit, the trigger signal could be exchanged for interlocking with the sequence PLC CPU from the Linux PLC CPU via the FA bus on the PLC base module. Therefore, it is possible to share the interlock signal of the high-voltage stage with the Linux PLC CPU and sequence PLC CPU without going through the TCP/IP network, which improves the system reliability of the interlock feature successfully without lowering the conventional system usability.

References

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