Implementation of the TDC function in the GTO

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The field-programmable gate array (FPGA) has become a popular device and has been widely adopted for physics measurements[1] in recent years. An FPGA-based NIM logic module has been developed[2] called a Generic Trigger Operator (GTO). Advanced logic circuits have successfully been introduced in the GTO[3,4]. The present article describes the implementation of the time-to-digital converter (TDC) function in the GTO.

There are several attempts to develop the TDC function in FPGAs[5,6]. The conversion time of a conventional TDC is typically 10–100 μs, while that of an FPGA-based TDC is only tens of nanoseconds. The block diagram of the TDC function in an FPGA is shown in Fig. 1. The shaded triangles are delay units. FF denotes to the flip-flop component. The coarse timing value is obtained using the global clock. When a 50-MHz clock is applied, the coarse timing value will be a 20-ns step. To obtain the fine timing value beyond the clock frequency, the tapped delay line (the cascade chain of the delay units in Fig. 1) and FF array are used. An input signal is delivered to the FF components whenever the signal passes through the delay units. The value of the FF array is latched by the global clock which achieves mostly equal-length wiring. The encoder seeks transitions of "0→1" and "1→0" in the FF array. The former transition corresponds to the leading edge of the input signal, and the latter one is the trailing edge. Thus, this TDC is capable of measuring both the edges of the signal at the same time. In this work, the look-up-table (LUT) and the carry-logic (CL) components are adopted as a delay unit. These are called as LUT-DL TDC and CL-DL TDC, respectively. The LUT-DL TDC uses 45 LUT components and a 50-MHz global clock. The CL-DL TDC consists of 113 CL components and a 162.5-MHz global clock. The conversion times are 40 ns (2 global clocks) for the LUT-DL TDC and 18.5 ns (3 global clocks) for the CL-DL TDC.

The differential non-linearity (DNL) has been measured to investigate the performance of the developed TDC function. The linearity of the coarse timing is quite good as the global clock is generated from the quartz resonator that has a frequency stability of 10^{-6}. However, the linearity of the fine timing depends on the variation of the propagation delay of the LUT/CL components and the wiring length in the FPGA. Figure 2 shows the result of the DNL measurement for the fine timing. The measurement method is the same as that in Ref. 6. The least significant bit (LSB) of the LUT-DL TDC and CL-DL TDC is 446 ps and 54.6 ps, respectively. The bin number corresponds to the n-th LUT/CL components. The LUT-DL TDC has a good performance because the DNL is much less than 1 LSB in any bin. However, some bins of the CL-DL TDC reach ±1 LSB, which implies there are missing values in the converted result. This DNL for the CL-DL TDC may be improved by fine tuning the wiring length in the FPGA.

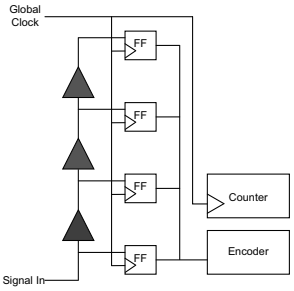

Fig. 1. Block diagram of TDC in the GTO.

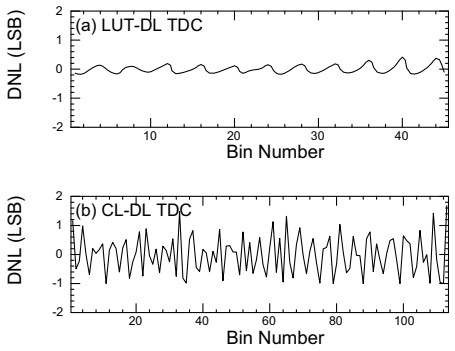

Fig. 2. The differential non-linearity of the developed TDC.

Two types of TDC functions have successfully been introduced in the GTO. Its conversion time is very fast and the linearity is reasonable. Based on this result, the particle-identified trigger for future BigRIPS experiments will be established by analyzing the time-of-flight, position and delta-E information in the GTO.

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