Development of sensor prototype for sPHENIX Silicon Tracker

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sPHENIX is a new detector at RHIC[1], which will be used for measuring jets, direct photons and Upsilon. The detector has electronmagnetic and hadronic calorimeters to measure jets and a high precision tracker. The tracker is contained inside a 1.5 T superconducting solenoid which was previously used for Babar experiment at SLAC.

We aim to construct a large silicon tracker for sPHENIX[2] and are working on the research and development of the silicon detector. The tracker consists of three tracking stations (from inner to the outer, called S0, S1 and S2) covering $-1 < \eta < 1$ and $\Delta\phi = 2\pi$.

The basic building block of the silicon tracker is a sensor module, which consists of a sensor, two High Density Interconnects (HDIs) for read-out, and mechanical support. We are currently developing a prototype of the silicon module used for the S1 layer. In this paper we report the status of a prototype silicon strip sensor for the S1 silicon module. The status of HDI is reported by another paper[3].

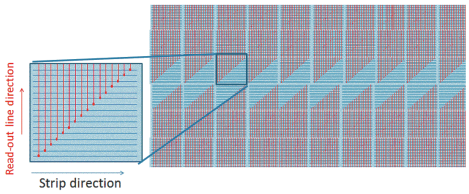

Fig. 1. Conceptual design of the S1 strip sensor.

Figure 1 illustrates the conceptual design of the S1 sensor. The sensor is a single sided, AC coupled sensor. The active area of the sensor, 96 mm (z) × 45.5 mm (ϕ), is divided into 10 × 6 blocks. Each block has 128 short strips that are 58 μm in pitch and 9.6 mm long, and run parallel to the z (beam) direction. In Fig. 1, the strip runs horizontally. The read-out lines of the strips, indicated by red lines in the figure, run perpendicular to the strips and bring the signals to the read-out chips placed at the upper and the lower edge of the sensor. The upper and the lower 3 blocks are connected upwards and downwards, respectively. This arrangement reduces the channel count to save the cost of the detector. Although signals in the 3 strips are combined and cannot be distinguished in the read-out chip, the offline track reconstruction program should distinguish the correct hit strip by requiring a good χ^2 for tracks fitted to all layers simultaneously. The probability of misidentifying the hit strip is low owing to the expected low channel occupancy. The occupancy is $\simeq 0.2\%$ even in central Au+Au collisions.

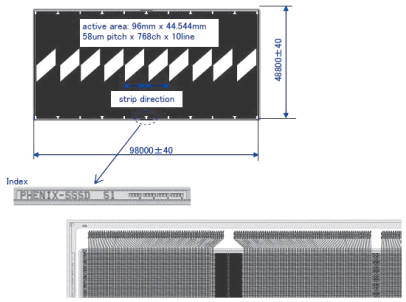

Fig. 2. A drawing of the S1 prototype sensor.

FPHX chip, which is used for FVTX silicon detector of PHENIX, is utilized to read-out the sensor. The read-out pad pitch of the sensor is thus matched to that of FPHX chip (75 μm). FPHX chip has low power consumption, about 64 mW per chip, which reduces the need for cooling for the sensor module. A FPHX chip has 128 ch and is used to read-out 3 blocks that are combined together. A total of 20 FPHX chips, 10 at the upper edge and 10 at the lower edge, are used to read-out one sensor.

The sensor will be manufactured by Hamamatsu Photonics Co. (HPK). Figure 2 is a part of a design drawing of the sensor made by HPK. Two sensors will be fabricated on one 6-inch wafer. The size of the sensor is maximized to fabricate two sensors on a 6-inch wafer.

We will produce two types of sensors in the same design. One is 320-μm thick, which is the standard thickness of wafers that HPK uses. The other one is 240-μm thick, which is made by thinining the 320 μm sensor. The thinner sensor results in lower scattering of charged particle and thus improve the momentum resolution of tracks. However, the signal generated by a hit will be reduced. We will evaluate the S/N ratio for MIP particles for both types of sensors to determine which one we will use for the production.

The design of the sensor at HPK has been complete and they are manufacturing the sensors. We expect the delivery of the sensors by early 2016.

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References

1) sPHENIX preliminary Conceptual Design Report (2015).
2) I. Nakagawa, in this report.
3) G. Mitsuka, in this report.