Evaluation of single-event damages on Silicon Carbide (SiC) power MOSFETs

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Silicon carbide (SiC) is the material used in next generation semiconductor devices that is applicable to higher voltage and temperature applications because of the inherent wide energy band-gap of 3.26 eV.[1)] In addition, saturated electron velocity is considerably fast in the SiC material. Therefore, SiC devices can operate in ultra-high frequency applications.[2)] If the SiC material is used in power devices instead of Si, these devices can achieve higher efficiency and lower loss.[3)] In our study, we investigated in detail the fatal destruction mode called Single-Event Burnout (SEBs) on commercial SiC power MOSFETs with the radiation effect during heavy-ion irradiations in space.

A single ion incidence into the device generates some amount of charge according to the Linear Energy Transfer (LET) value of the ion, and the charge can be amplified in the device using mechanisms such as avalanche multiplication. Finally, the charge is collected at the drain terminal and can be measured using a charge sensitive amplifier (CSA). The input charge range and the output voltage of CSA are 0.5 - 50 nC and 0.1 mV - 10 V, respectively. For the cases where the amplification level increases exponentially with the applied voltage to the sample device, the Energetic Particle Induced Charge Spectroscopy (EPICS) is more suitable. EPICS is specially designed for the pulse-height analyzer (PHA) system that is used to analyze the charge collection characteristics in semiconductor devices.[4)] It can measure a wide range of charges using a logarithmic scale. The block diagram of the EPICS system is shown in Fig. 1.

SiC power MOSFETs used in this study were commercial devices. The maximum ratings for the drain-Source breakdown voltage, continuous drain current, and the drain-source on-state resistance are 1200 V, 24 A, and 220 mΩ, respectively.

The test was performed at room temperature by irradiation with a Kr-ion beam of 713 MeV using the RIKEN RILAC+RRC. Fluence was set to 1×10^5 ions/cm^2 at the chip surface. The drain bias voltage, V_{DS}, was increased at an interval of 50 V. The gate voltage, V_{GS}, was set to 0 V to force the devices to enter the OFF state.

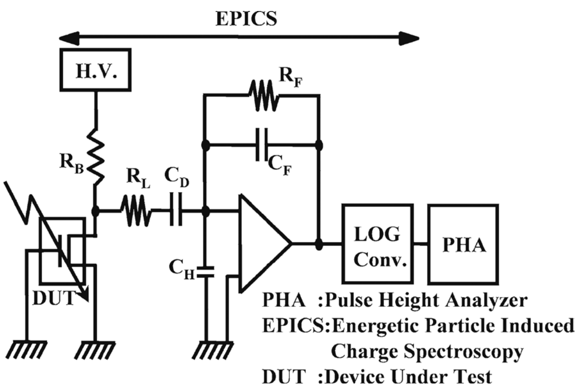

Fig. 1. Block diagram of EPICS system.

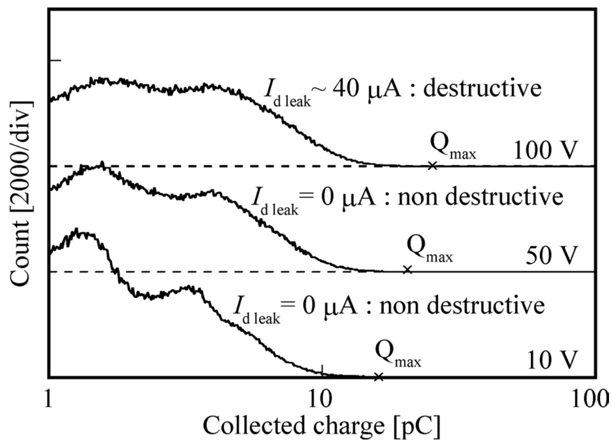

Fig. 2. Collected charge spectra by Kr ion irradiation using the EPICS system.

Figure 2 shows the EPICS spectra on SiC power MOSFETs of Kr-ion irradiation. The cross marks Q_{max} indicate the maximum collected charge for each spectrum. There were two peaks on each spectrum similar to the one of Si power MOSFETs.[4)] At the drain voltage of 100 V, the device was damaged because the leakage current was more than the maximum rated zero gate voltage drain current of 10 μA. In Si power MOSFETs, a high energy collected charge peak Q_{max} of more than 10^5 pC was observed when SEB occurs. However, in SiC power MOSFETs, permanent increase of the leakage current was observed at the drain voltage of 100 V; However, no high SEB peak was observed up to the voltage level, and the maximum collected charge was less than 100 pC. This behavior is the same as our previous study on SiC Schottky barrier diodes.[5)] This fact suggests that the mechanism of SEB was different between SiC power MOSFETs and Si power MOSFETs. Therefore, it is necessary to perform additional experiments to understand the SEB mechanism of SiC power MOSFETs.

References

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