

## SPYBOX: Clock Monitoring at the GET Electronics

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The SPYBOX is a device that measures the time differences between the clock signals of the various AsAd boards (ASIC Support and Analog-Digital conversion) at the GET electronics (General Electronics for TPC)<sup>1)2)</sup> in order to monitor the clock synchronisation. It will be used at SPiRIT - the TPC at the SAMURAI experiment.

At the GET electronics a total number of 120 AsAd boards are available, enabling GET to read out more than 30000 channels of a TPC. At each AsAd board, there are two inspection lines available which can be used to monitor various internal signals such as clock signals. These clock signals are fed into the SPYBOX.

For the SPYBOX two stages of multiplexer are implemented in FPGAs (see figure 1): At the first stage, 64 signals are multiplexed to two. Up to four of these FPGAs exist. The second stage reduces the remaining eight signals to two which are used as start and stop signal for an external TDC. Thus, a total number of 256 clock signals can be monitored, slightly exceeding the 240 inspection lines available in GET.

The time difference between the two signals is read from the TDC by a microcontroller which also serves as communication interface to the user's computer.

So far, two prototypes have been developed. The first prototype<sup>3)</sup> houses all components on one board. Tests with clock signals show that the principle is feasible and yield a maximum skew of about 0.5 ns (see figure 2).

Nevertheless, this prototype has some drawbacks. For instance, the connectors as implemented on the board are not compatible with the AsAd board, and only about half the total number of clock signals can be processed. Moreover, the large size of this board turns out to be unhandy. By this, the need for a second prototype arose.

The second prototype is compatible with the AsAd board. It has a compact and modular design consisting of an own board for each stage of multiplexer. Thus, it allows the use of a reduced setup – for example at SPiRIT where only about 50 AsAd boards are used. Additionally, the second prototype leaves space for further developments. One of the inspection lines at AsAd is for example bidirectional. It either outputs internal signals or receives external trigger signals for the AsAd pulse generator. The design of the second board accounts for the bidirectional line.

One additional feature of the second prototype concerns the timing resolution. As this prototype has a significant number of integrated circuit chips, the indi-

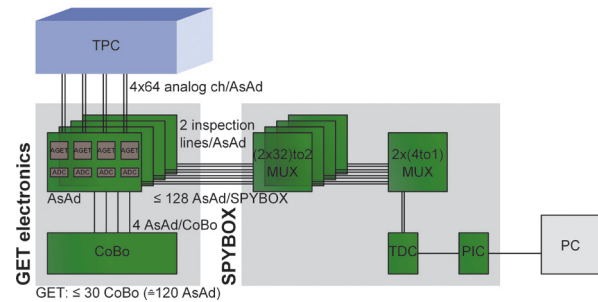


Figure 1. Schematics of GET and SPYBOX

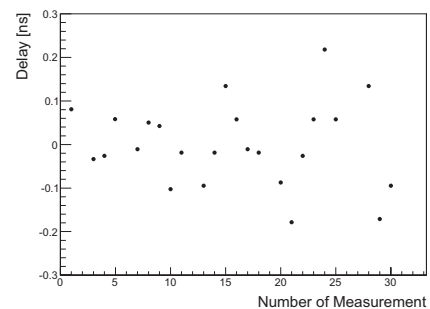


Figure 2. Time difference between two channels fed by the same clock signal corrected by the clock period

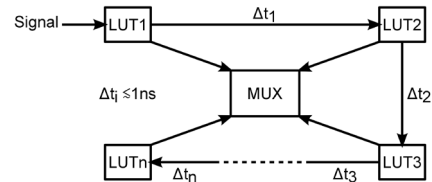


Figure 3. Delaying an individual channel by LUTs

vidual channels are prone to experience different travel times. To improve the timing resolution individual delay can be added to each channel compensating for the different travel times. This is done inside the FPGAs by a chain of LUTs (look-up-tables) which leads to freely selectable wire delay (see figure 3). First tests of the delay adjustment implemented in the FPGA yield additional delays of (0.7 to 0.8) ns per LUT. The time difference between two channels can be measured with a standard deviation of slightly less than 0.05 ns.

Currently, the second prototype is about to be finalized and will be evaluated afterwards.

### References

- 1) E. C. Pollacco et al.: LoI for GET - General Electronics for TPC (2008)
- 2) <http://www.actar-get.cea.fr>
- 3) K. Urano et al.: RIKEN Accel. Prog. Rep. **46**, 152 (2013)

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